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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,506	05/02/2005	Bijo Thomas	IN 020004	4348

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EXAMINER	
PHAN, DEAN	

ART UNIT	PAPER NUMBER
2182	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,506	THOMAS, BIJO	
	Examiner	Art Unit	
	Dean Phan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *07 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation "data input and/or output", e.g. line 3, in claims 1 and 11 is indefinite. It is unclear whether the applicant intends to use either "and" or "or" in the claim limitation. Correction/Clarification is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-4, 6-8, 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joffe et al (US Pat# 6,205,523), in view of Buck-Gengler (US Pat# 5,777,628).

As to claim 1, Jofffe et al teach a data processing apparatus (fig. 15), comprising:

a plurality of data processing units (col 11 lns 30-32), each having an address output (Fig 1; The address output connects to control bus 164) and a data input and/or output (The data output connects to memory buffers 130);

a plurality of memory units (Fig 15 memory 110_A-D & 110'_A-D), each having an address input (Fig. 1 memory 110; address input A) and a data input and/or output (Data input D);

a switching unit (Fig 15, memory bus switch 1120) comprising:

first selectable connections between the data input and/or outputs of the processing units and selectable ones of the data input and/or outputs of the memory units and second selectable connections from the address outputs of the processing units to the address inputs of selectable ones of the memory units (Fig. 1, fig 15, col 12 lns 12-18; *data bus and address and control bus are selectable between the processing unit 122 and 110A-D & 110'A-D in order to switch*),

a state holding element (Fig 1,5 address Gen 170; *Address gen 170 controls address switch function*) for controlling the first and second selectable connections, in order to switch the first and second selectable connections between pluralities of memories (*110A-D*) and its mirror images (*110'A-D*).

Joffe et al do not teach a detection unit arranged to detect repetitions of an identical address output by the at least one of the processing units and the state holding element having an input coupled to the detection unit, in order to switch the first and second selectable connections in response to the detection of a new one of said repetitions so that identical addresses from the data processing units map to different

ones of the memory units. However, in the same field of art, Buck-Gengler teach a method to avoid address collision (abstract) when previous access and current access have the same memory address (col 1 lns 35-40). The method comprises a detection unit (Fig 2 collision detector 214), coupled to the input of the memory controller (Fig 2; *Memory controller functions as a state holding element which input/outputs data to/from memory*). The detection unit arranged to detect repetitions of an identical address output by the at least one of the processing units (col 1 lns 49-60). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement the teachings of Buck-Gengler in the teaching of Joffe et al, by using a detection unit arranged to detect repetitions of an identical address output by the at least one of the processing units and the state holding element having an input coupled to the detection unit, in order to switch the first and second selectable connections in response to the detection of a new one of said repetitions so that identical addresses from the data processing units map to different ones of the memory units (*Since the mirror memory 110' A has identical addresses as the memory 110 A*), in order to avoid address conflict and obtain higher performance (*see* col 1 lns 34-40).

As to claim 3, all limitations are in claim 1, wherein the detection unit comprises an address comparator (Buck, Fig 2 collision detector 214) arranged to detect whether addresses from the address output of a first one of the data processing units fall in a range of one or more addresses associated with the memory units (Buck, col 1 lns 35-40; *Detecting/Comparing whether the second address fall into the range of the first address which associates with the memory units*), and to generate a detection signal

indicating the new one of said repetitions each time when one of the addresses from the address output of the first one of the data processing units has output addresses in said range (Buck, col 1 lns 39-42; *To flush the queue, the detection unit generate a signal to the controller*) a certain number of times (*certain number of times is 1*).

As to claim 4, all limitations are in claim 3, wherein said certain number is one (Buck, Col 1 lns 34-40; *Certain number of times is 1*), and wherein said range is a subset of one or more of the addresses associated with the memory units (*The comparing address is the subset of more than one addresses associated with the memory units*).

As to claim 6, all limitations are in claim 1, wherein the detection unit comprises an access memory (Buck, col 1 lns 49-51; *Associative memory*) for the at least one of the data processing units. The access memory comprising locations for a plurality of the addresses that address locations in the memory units that are addressable by the first one of the data processing units (Buck, col 1 lns 51-57), the access memory being arranged to record access to the locations in the memory units (*the associative memory stores the address of each access*), the detection unit being arranged to generate a detection signal indicating the new repetition in dependence on whether the access memory indicates that an address supplied by the first one of the processing units has been supplied before during the repetition.

As to claim 7, all limitations are in claim 6, wherein the detection unit generates the detection signal when the at least one of the data processing units outputs an

address for which the access memory has previously recorded access after a previous detection of said new repetition (Buck, col 1 lns 35-55).

As to claim 8, all limitations are in claim 6, wherein the detection unit generates the detection signal when the at least one of the data processing units has executed more than a certain number of addresses for which the access memory indicates that the address has not been supplied previously during the repetition (*the processing units continues accessing more than one address unlessl the repetition is detected*).

As to claim 10, all limitations are in claim 1, wherein the detection unit is arranged to perform the detection of repetitions involving repetition of read and/or write control signals from at least one of the processing units (Col 23-40; *To access is to read or write*).

As to claim 11, all the same elements of claim 1 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 1 applies equally as well to Claim 11.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joffe et al (US Pat# 6,205,523), in view of Buck-Gengler (US Pat# 5,777,628), in further view of Andrew S. Tanenbaum ("Structured computer organization").

As to claim 2, Joffe et al and Buck-Gengler teach a data processing apparatus according to Claim 1, wherein hardware (Buck, col 1 lns 34-60) but do not teach the criterion for detecting the new one of the repetitions is programmable under the control of a program executed by the apparatus. However, in the same field of art, Andrew S. Tanenbaum teaches the concept of choosing between hardware and software. Andrew

S. Tanenbaum teaches any instruction executed by the hardware can be simulated in software (page 11 lns 13-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Andrew S. Tanenbaum in the teaching of Joffe et al and Buck-Gengler by implementing the apparatus wherein the criterion for detecting the new one of the repetitions is programmable under the control of a program, in order to provide the flexibility of the system and less cost (*see page 11 lns 13-19*).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joffe et al (US Pat# 6,205,523), in view of Buck-Gengler (US Pat# 5,777,628), in further view of Packer (US Pat# 5,551,054).

As to claim 5, Joffe et al and Buck-Gengler teach a data processing apparatus according to Claim 3, but do not teach said certain number is greater than one and the apparatus comprising a counter for counting a counted number of the addresses from the address output of the first one of the data processing units in said range at least until said certain number. However, in the same field of art, Packer teaches a method of memory data transfer (abstract). Packer realizes that increasing the size of data to be transferred will reduce the overhead clock cycles (col 7 lns 45-54). The size of transferred data block is tracked by a counter (col 4 lns 10-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement the teachings of Packer in the teaching of Joffe et al and Buck-Gengler, *by transferring a block of data in a range of memory, instead of a byte in single address*, so that a certain number is greater than one and the apparatus comprising a counter for counting a

counted number of the addresses from the address output of the first one of the data processing units in said range at least until said certain number. The motivation of the implement is to reduce the overhead clock cycles and to increase the speed of data transfer from/to memory (*see Background, col 1 ln 55-col 2 ln 29*).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joffe et al (US Pat# 6,205,523), in view of Buck-Gengler (US Pat# 5,777,628), in further view of Litt (US Pat# 6,816,989).

As to claim 9, Joffe et al and Buck-Gengler teach a data processing unit according to Claim 1, wherein said plurality of memory units (18a,b) comprises three or more memory units (Joffe, fig 5), the state holding element controlling the switching of the first and second selectable connections (fig. 1 address gen logic 170), so that identical addresses from the data processing units map to different ones of three or more of the memory units during successive repetitions. Joffe et al and Buck-Gengler do not teach the addresses cyclically map to different one of more of memory units. However, in the same field of art, Litt teaches a buffer controller (fig 2 arbitration logic 250) which switches between pluralities of buffer. The controller is implemented a round-robin approach (cyclically map) where it will alternatively select each buffer. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Litt in the teaching of Joffe et al and Buck-Gengler in order to distribute the load balance equally to each memory units in the system (*see col 12 lns 35-43*).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior arts are from the same field of memory data transfer.

US# 4,920,484	Ranade, Abhiram G.
US# 2004/0139234	Quach et al.
US# 2003/0172149	Edsall et al
US# 5,522,045	Sandberg, Jonathan

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dean Phan whose telephone number is (571) 270-1002. The examiner can normally be reached on Mon - Thu; 9:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

dp

6/21/07